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S P E C I F I C A T I O N

**AN APPARATUS AND METHOD FOR A CONFIGURABLE MIRROR FAST
SENSE AMPLIFIER**

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to Italian Application Serial Number 03A000132, filed February 25, 2003.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0002] The invention relates to memory. More particularly, the invention relates to configuring a mirror sense amplifier in order to create a reference current by which to read the state of flash memory cells.

2. The State of the Art

[0003] A system for reading flash memory typically employs a differential sense amplifier to compare the amount of current flowing through a reference cell to a selected memory cell. A sensing circuit determines if the selected memory cell has logic 1 or logic 0 stored therein based on the comparison.

[0004] When the amount of current flowing through the reference cell is larger than the amount of current flowing through the selected memory cell then logic value 0 (programmed) is read from the memory cell. When the amount of current flowing through the reference cell is smaller than the amount of current flowing through the selected memory cell then logic value 1 (erased) is read from the memory cell.

[0005] A current reference, generally half the current of an erased cell (logic value 1), enables the system to determine, through comparison with the current of the memory cell, what logic value is stored in the selected memory cell. The current reference is typically set so that the system distinguishes between programmed and erased states.

[0006] A reference cell generates the reference current. The reference cell is located in an array outside the memory array in order to avoid the write and erase cycles that modify the threshold of the reference cells. The reference current is carried around the chip by a system of current mirrors.

[0007] Figure 1 illustrates system 10 wherein local mirror 12 mirrors a reference current inside sense amplifier 15.

[0008] Sense amplifier 15 has bias circuit 17 to bias a bit line. Reference voltage generator 19 provides a voltage level, usually generated from the reference cell current, for comparator 21. Comparator 21 determines if the reading array cell is erased or programmed.

[0009] Memory access time depends on how rapidly the reference current circuit can turn on. Node 16 is precharged at a reference value and allowed to evolve. Equalization circuitry (not shown) permits the evolution of charge at node 16. The equalization circuitry produces a load effect on a signal on line 18.

[0010] One drawback to the aforementioned design is that since the signal on line 18 is the same for all sense amplifiers 15, the load effect may reduce the performance for fast memory access. Additionally, the added load effect of the equalization circuitry increases memory access time. Furthermore, frequent reading of the memory cells may change the threshold voltages of the reference cells and therefore compromise their reliability.

[0011] The minimum Vcc for circuit 20 used to bias the reference cell depends on p-channel transistor 11 in diode configuration and on cascode 13 that biases the reference bit line at about 1V, so that if transistor 11 is conductive

enough then its V_{GS} can be approximated to its threshold V_{thP1} and minimum V_{cc} is

$$V_{cc} = V_{thP1} + 1V + V_{dsatN1}.$$

In modern, low voltage circuits the minimum V_{cc} should be as low as possible.

BRIEF DESCRIPTION OF THE INVENTION

[0012] The invention provides a method and apparatus for a configurable mirror sense amplifier. A configurable array of selectable transistors whereby one or more transistors serves as a current reference for memory cells in a flash memory device. The current reference is compared to the current in a memory cell and a logic level of 0 or 1 is read from the memory cell based on whether the current in the memory cell is greater than or less than the current reference.

[0013] The array is configured in order to provide a suitable current reference level that allows the system to distinguish between current in the memory cell intended to represent logic level 0 and current intended to represent logic level 1.

[0014] The array is configured by either selecting one or more transistors to serve as the current reference, or varying the voltage applied to the gate at least one of at least one transistor in order to vary the amount of current flowing through the transistor, or a combination of selecting and varying.

BRIEF DESCRIPTION OF THE FIGURES

[0015] FIG. 1 is a schematic diagram illustrating a prior art memory cell content reader.

[0016] FIG. 2 is a schematic diagram illustrating one embodiment of the invention.

[0017] FIG. 3 is a schematic diagram illustrating one embodiment of the invention.

[0018] FIG. 4 is a flow diagram illustrating a method of configuring a mirror sense amplifier.

[0019] FIG. 5 is a flow diagram illustrating a method of configuring a mirror sense amplifier.

[0020] FIG. 6 is a flow diagram illustrating a method of configuring a mirror sense amplifier.

DETAILED DESCRIPTION OF THE INVENTION

[0021] Persons of ordinary skill in the art will realize that the following description of the invention is only illustrative and not in any way limiting. Other embodiments of this invention will be readily apparent to those skilled in the art having benefit of this disclosure.

[0022] FIG. 2 illustrates one embodiment of the invention. Bitline current 100 is compared to one or more currents from reference circuit 102. Configurable transistors 104 (or reference transistors) are biased with the same reference voltage. The reference voltage is internally generated, stable and independent from power supply and temperature variations. In one embodiment, the reference voltage is a bandgap reference (not shown).

[0023] Current passing through transistor 112 is used as a reference current. The amount of current passing through transistor 112 is a function of how many of transistors 104 are biased to an active (conducting) mode. Transistors 104 are in a configurable array and one or more of transistors 104 are biased to an active mode in order to provide a desired current through transistor 112 and therefore a desired reference current. In one embodiment, each transistor 104 in the array is part of a group. Current through transistors 104 is selected by biasing transistors 106. For example, transistor group 103-1 is comprised of transistors 104-1 and 106-1. In order to select current passing through transistor 104-1, which is also the same

current passing through transistor 106-1 and group 103-1, transistor 106-1 is biased to an active mode. Transistor group 103-2 is comprised of transistors 104-2 and 106-2. In order to select current passing through transistor group 103-2, transistor 106-2 is biased to an active mode. Transistor group 103-3 is comprised of transistors 104-3 and 106-3. In order to select current passing through transistor group 103-3, transistor 106-3 is biased to an active mode, and so on. The selected transistor group is rapidly switched on. Load effects due to transistor groups 103 allow faster access time.

[0024] The sum of the current through transistor groups 103 is the same as current through transistor 112. Current through transistor 112 is mirrored by mirror transistor 113 and compared with current in a selected memory cell, for example memory cell 110. After selecting one or more transistor groups 103, current through those groups, mirrored by transistor 113, is compared to memory cells. If current in memory cell 110 is greater than current in selected transistor group 103 then a logic level of 1 is assigned to memory cell 110. Conversely, if current in memory cell 110 is less than current in selected transistor group 103 then a logic level of 0 is assigned to memory cell 110. If more than one transistor group 103 is selected then the sum of the current through the selected groups is compared to the current in the memory cell. In one embodiment, transistors 104 are N-channel transistors operated in saturation.

[0025] The minimum for Vcc

$$V_{CC} = V_{TH} + V_{NODE1}$$

where V_{TH} is approximately the threshold voltage of transistor 112 and V_{NODE1} is the voltage across node 114 and ground. A lower minimum Vcc allows for a broader range of low voltage applications for the invention in comparison to circuits having a higher minimum Vcc.

[0026] Sense amplifier 115 includes circuit 116 for biasing bit line 100 and transistor 113 that forces a reference current on bit line 100. Reference voltage generator 118 provides a voltage level typically generated from the reference cell current. Comparator 120 determines if the memory cell is erased or programmed.

[0027] With respect to Figure 2, a reference current is typically established through experimentation. The reference current should be sufficiently above the current in the memory cell that represents a logic level of 0 and sufficiently below the current that represents a logic level of 1 so that incorrect values are not read from flash memory.

[0028] Transistor 113 mirrors the current passing through transistor 112. Once a suitable reference current is established, the current passing through

transistor 112 and will be compared, through the mirror of transistor 113, to current within memory cells.

[0029] One method of establishing the reference current is with signals 108. Signals 108 activate each group based on current values passing through the respective transistors. For example, if current passing through transistors 104-1 and 104-2 provides a suitable reference current, then signals 108-1 and 108-2 will activate transistors 106-1 and 106-2. If current passing through transistor 104-4 provides a suitable reference current then signal 108-4 will activate transistor 106-4. One skilled in the art will recognize that each group of transistors by itself may provide a suitable reference current, and that other combinations of groups may provide suitable reference current as well. One skilled in the art will also recognize that fewer and more groups may be used and that this example applies to the embodiment illustrated in Figure 3 as well.

[0030] In one embodiment, this configuration occurs during device testing and is not repeated. In another embodiment, this configuration occurs during power-up for the circuit.

[0031] Another method of adjusting the reference current is by adjusting the voltage on signal 130, which couples to the gate of each of transistors 104. Changing the voltage on signal 130 will change the amount of current flowing

through transistors 104. One skilled in the art will recognize that this method applies to the embodiment in Figure 3 and that a combination of this method and the previous method may be used.

[0032] Figure 3 illustrates one embodiment used to avoid Early effect. The Early effect depends on the shortening of the effective channel length in the saturation region caused by VDS being greater than the VDSAT limit. In this condition, the depletion region around the drain junction becomes wider, causing the standard drift transport equations to be replaced by more complex equations. The effect becomes more pronounced as channel length shortens.

[0033] Cascode structure 300 biases node 302. In one embodiment, bit line regulator 304 biases matrix bit line 306 at 1V while cascode structure 300 biases voltage at node 302 in order to avoid Early effect and may be lower than the voltage at node 306.

[0034] The voltage minimum for V_{CC} in the circuit of Figure 3 is

$$V_{CC} = V_{TH} + V_{NODE2} + V_{DS}$$

where V_{TH} is the threshold voltage of transistor 309 and V_{NODE2} is the voltage across node 302 and V_{DS} is the drain-to-source voltage across transistor 308. In one embodiment V_{NODE2} is less than 1V. As previously stated, a minimum V_{CC}

lower for the invention compared to the prior art allows for a greater range of low voltage applications.

[0035] While a sense amplifier is not shown on Figure 3, those skilled in the art recognize that the circuit in Figure 3 can include a sense amplifier as shown in Figure 2.

[0036] Figure 4 is a flow diagram illustrating a method of configuring a mirror sense amplifier. In block 400, determining a current sunk by one or more reference transistors. In block 410, selecting a configuration at least one of at least one reference transistor based on the current sunk by the one or more reference transistors. In block 420, comparing the sum of the current with a cell current in a memory cell in the flash memory.

[0037] Figure 5 is a flow diagram illustrating a method of configuring a mirror sense amplifier. In block 500, adjusting the gate voltage in a reference transistor such that a current flowing through the reference transistor is a suitable current reference. In block 510, comparing the current with a cell current in a memory cell in the flash memory.

[0038] Figure 6 is a flow diagram illustrating a method of configuring a mirror sense amplifier. In block 600, selecting one or more transistors such that

the sum of the current flowing through the one or more transistors approximates a suitable current reference. In block 610, adjusting the gate voltage on at least one of at least one transistor such that the sum of the current flowing through the one or more transistors approximates a suitable current reference. In block 620, comparing the sum of the current with a cell current in a memory cell in the flash memory.

[0039] While embodiments and applications of this invention have been shown and described, it would be apparent to those skilled in the art that many more modifications than mentioned above are possible without departing from the inventive concepts herein. The invention, therefore, is not to be restricted except in the spirit of the appended claims.